SONY

CXA1372BQ/BS

RF Signal Processing Servo Amplifier for CD Player

Description

The CXA1372BQ/BS is a bipolar IC developed for RF signal processing (focus OK, mirror, defect detection, EFM comparator) and various servo control.

Features

- Dual ±5V and single 5V power supplies
- Low power consumption
- Fewer external parts
- Disc defect countermeasure circuit
- Fully compatible with the CXA1182 for microcomputer software

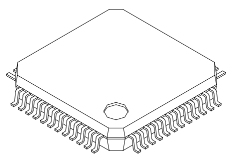
Functions

- Auto asymmetry control
- Focus OK detection circuit
- Mirror detection circuit
- Defect detection, countermeasure circuit
- EFM comparator
- Focus servo control
- Tracking servo control
- Sled servo control

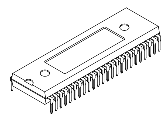
Structure

Bipolar silicon monolithic IC

CXA1372BQ
48 pin QFP (Plastic)



CXA1372BS
48 pin SDIP (Plastic)



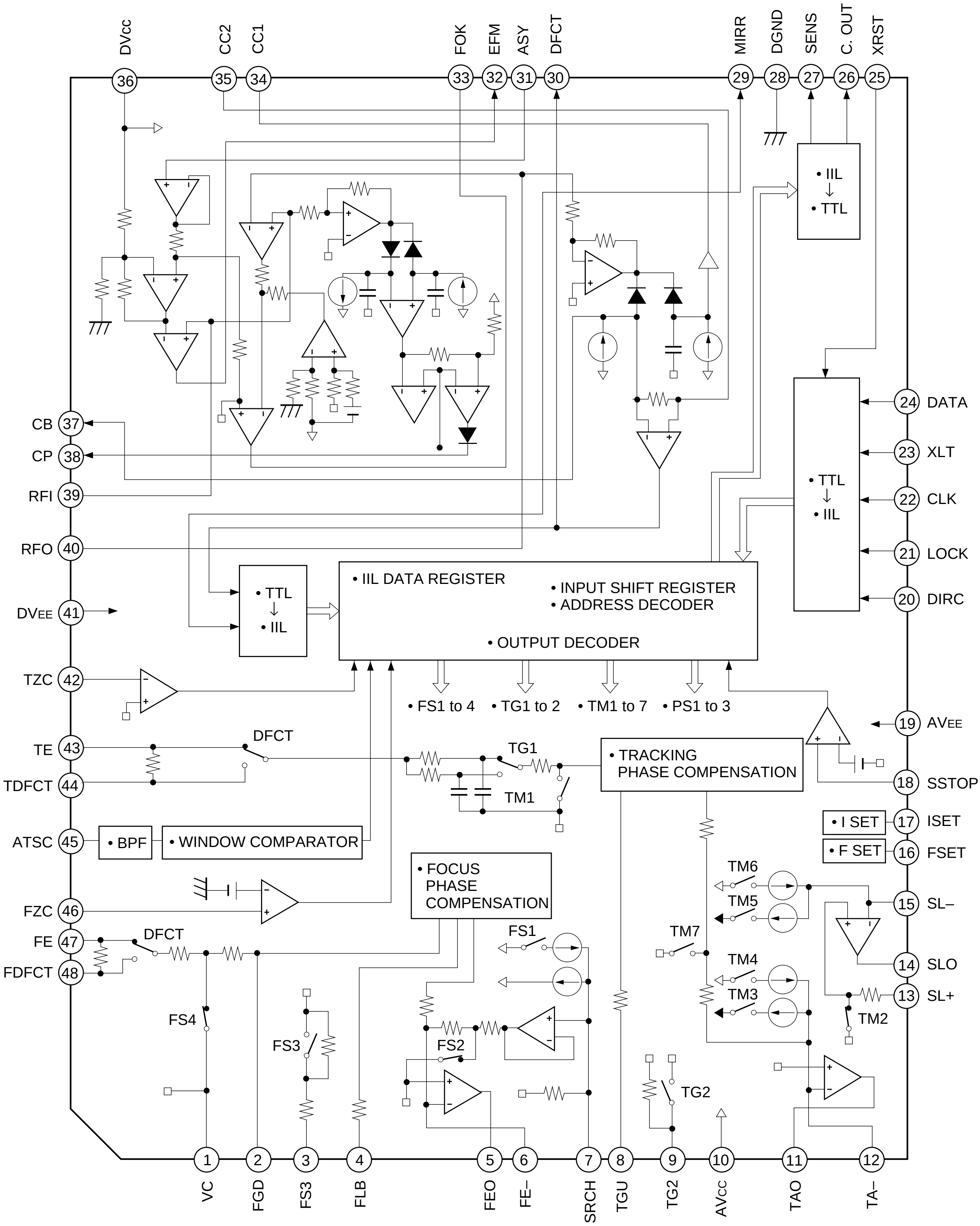
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	$V_{CC} – V_{EE}$	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	457 (CXA1372BQ)	mW
		833 (CXA1372BS)	mW

Recommended Operating Conditions

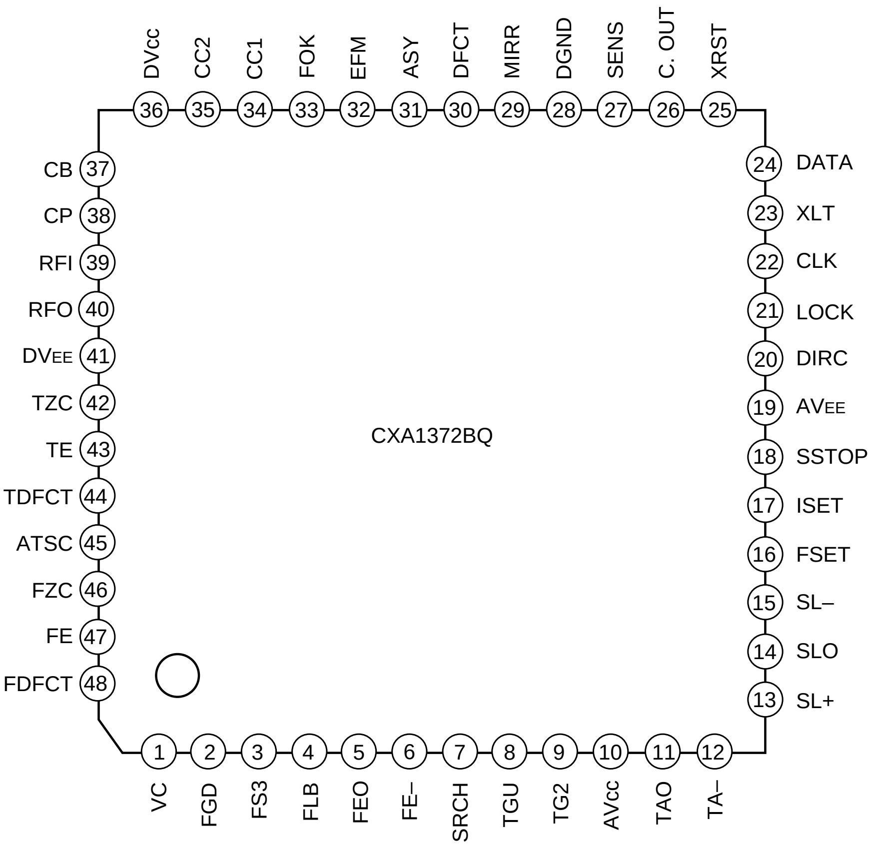
$V_{CC} – V_{EE}$	3.6 to 11	V
$V_{CC} – D_{GND}$	3.6 to 5.5	V

Block Diagram

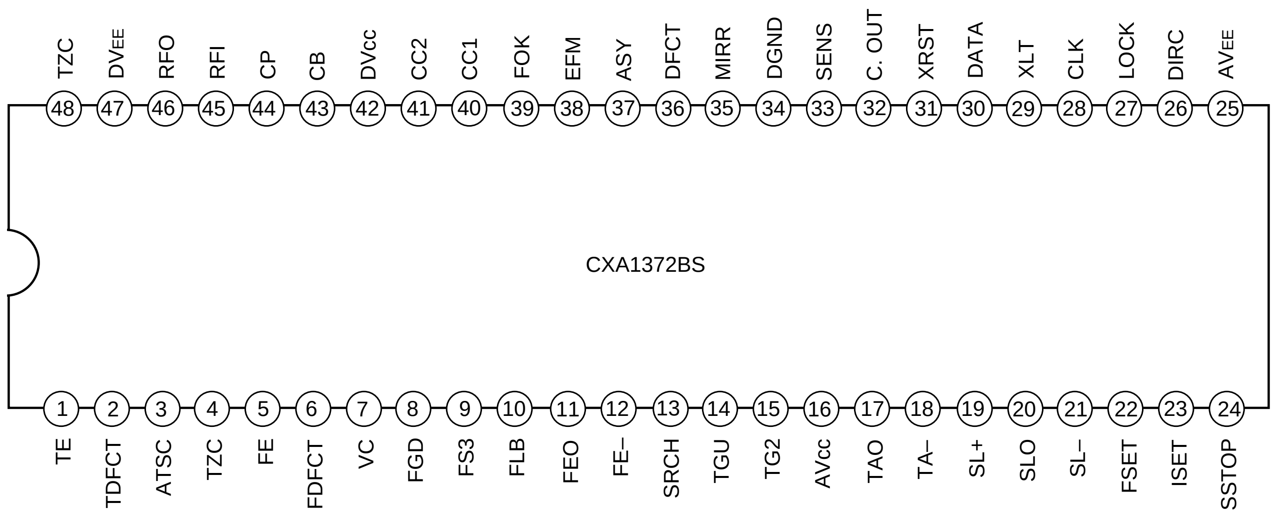


Pin Configuration

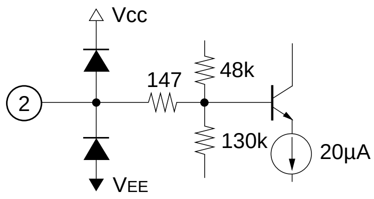
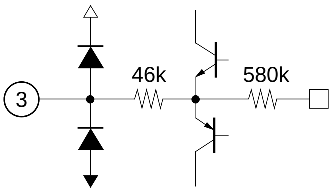
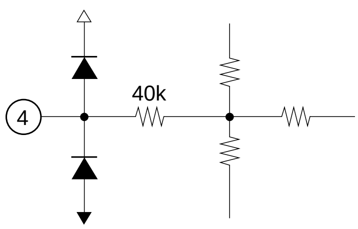
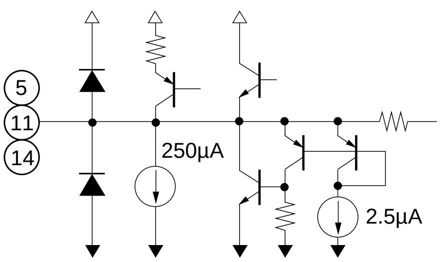
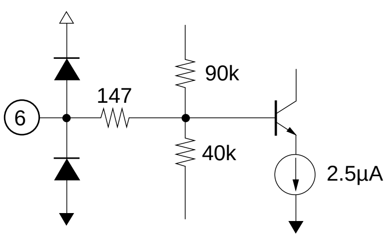
CXA1372BQ

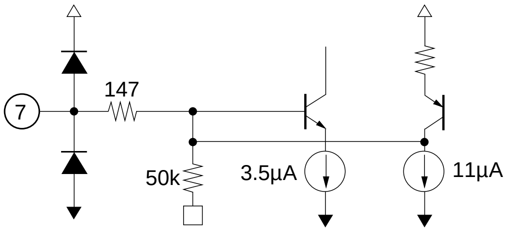
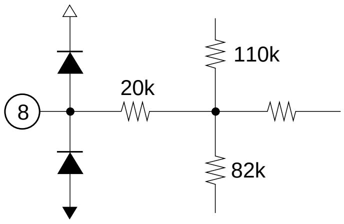
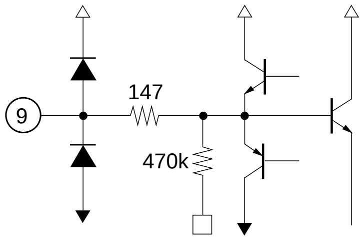
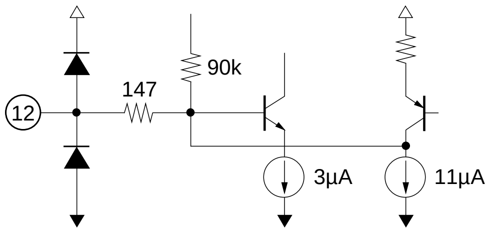
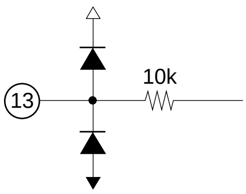
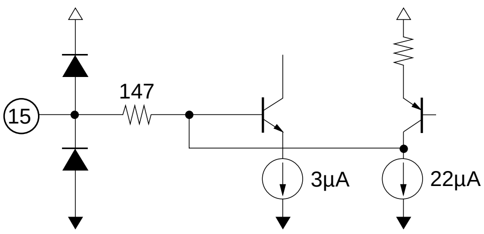


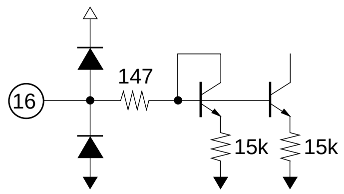
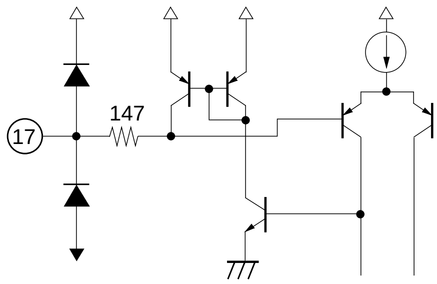
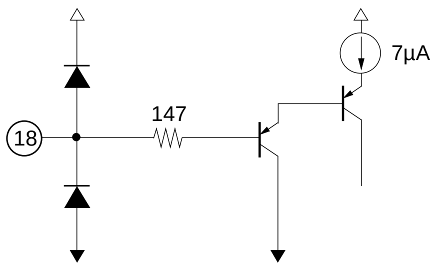
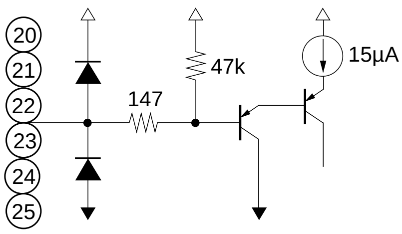
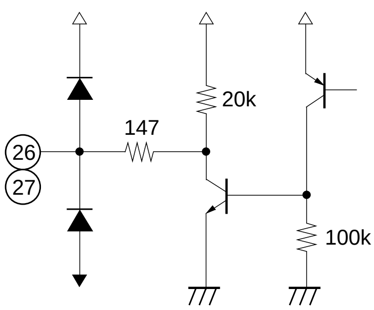
CXA1372BS

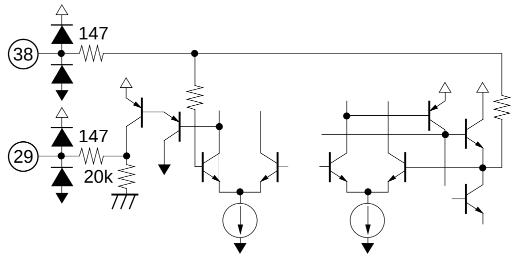
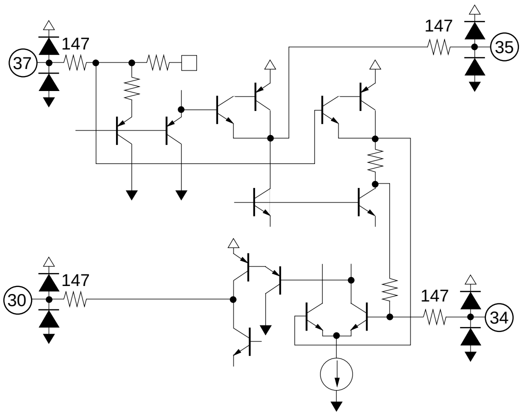
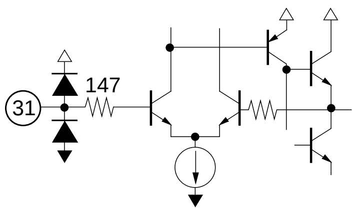
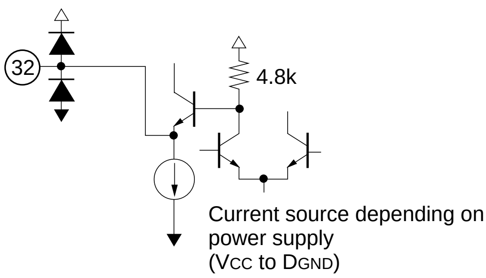
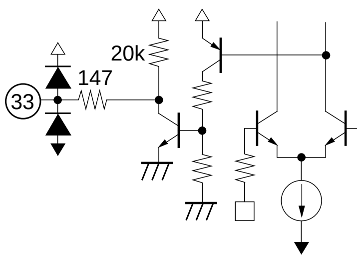


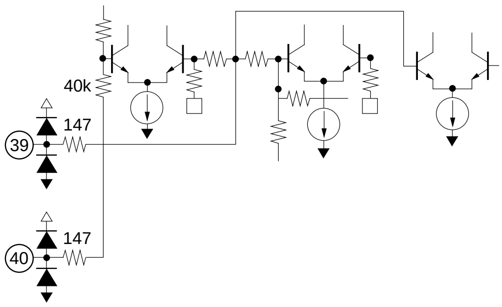
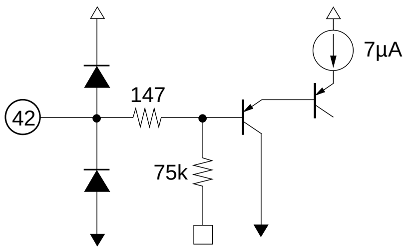
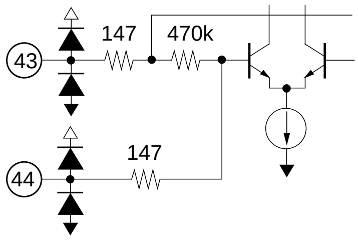
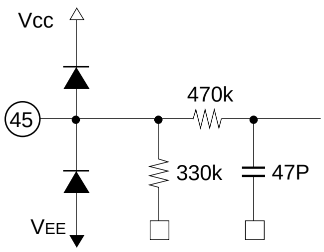
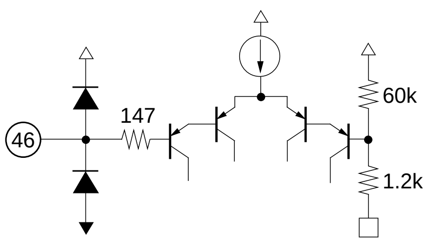
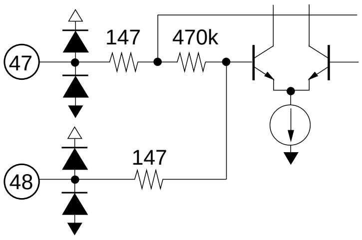
Pin Description

Pin No. Q	Pin No. S	Symbol	I/O	Equivalent circuit	Description
1	7	VC	I		Center voltage input. For dual power supplies: GND For single power supply: (Vcc + GND)/2
2	8	FGD	I		Connects a capacitor between this pin and Pin 3 to cut high-frequency gain.
3	9	FS3	I		The high-frequency gain of the focus servo is switched through FS3 ON and OFF.
4	10	FLB	I		External time constant to boost the low frequency of the focus servo.
5	11	FEO	O		Focus drive output.
11	17	TAO	O		Tracking drive output.
14	20	SLO	O		Sled drive output.
6	12	FE–	I		Inverted input for focus amplifier.

Pin No. Q	Pin No. S	Symbol	I/O	Equivalent circuit	Description
7	13	SRCH	I		External time constant for forming the focus search waveforms.
8	14	TGU	I		External time constant for selecting the tracking high-frequency gain.
9	15	TG2	I		External time constant for selecting the tracking high-frequency gain.
12	18	TA–	I		Inverted input for tracking amplifier.
13	19	SL+	I		Non-inverted input for sled amplifier.
15	21	SL–	I		Inverted input for sled amplifier.

Pin No. Q	Pin No. S	Symbol	I/O	Equivalent circuit	Description
16	22	FSET	I		Sets the peak frequency of focus tracking phase compensation.
17	23	ISET	I		Current is input to determine focus search, track jump, and sled kick level.
18	24	SSTOP	I		Limit SW ON/OFF signal detection for disc innermost track detection.
20	26	DIRC	I		Used for 1-track jump. Contains a 47kΩ pull-up resistor.
21	27	LOCK	I		At "Low" sled overrun prevention circuit operates. Contains a 47kΩ pull-up resistor.
22	28	CLK	I		Serial data transfer clock input from CPU. (no pull-up resistor)
23	29	XLT	I		Latch input from CPU. (no pull-up resistor)
24	30	DATA	I		Serial data input from CPU. (no pull-up resistor)
25	31	XRST	I		Reset input, reset at "Low". (no pull-up resistor)
26	32	C. OUT	O		Track number count signal output.
27	33	SENS	O		Outputs FZC, AS, TZC and SSTOP through command from CPU.

Pin No. Q	Pin No. S	Symbol	I/O	Equivalent circuit	Description
29	35	MIRR	O		MIRR comparator output. (DC voltage: 10kΩ load connected)
38	44	CP	I		Connects MIRR hold capacitor. Non-inverted input for MIRR comparator.
34	40	CC1	O		DEFECT bottom hold output.
35	41	CC2	I		Input for DEFECT bottom hold output with capacitance coupled.
30	36	DFCT	O		DEFECT comparator output. (DC voltage: 10kΩ load connected)
37	43	CB	I		Connects DEFECT bottom hold capacitor.
31	37	ASY	I		Auto asymmetry control input.
32	38	EFM	O		EFM comparator output. (DC voltage: 10kΩ load connected)
33	39	FOK	O		FOK comparator output. (DC voltage: 10kΩ load connected)

Pin No. Q	Pin No. S	Symbol	I/O	Equivalent circuit	Description
39	45	RFI	I		Input for RF summing amplifier output with capacitance coupled.
40	46	RFO	O		RF summing amplifier output. Check point of eye pattern.
42	48	TZC	I		Tracking zero-cross comparator input.
43	1	TE	I		Tracking error input.
44	2	TDFCT	I		Connects a capacitor for time constant during defect.
45	3	ATSC	I		Window comparator input for ATSC detection.
46	4	FZC	I		Focus zero-cross comparator input.
47	5	FE	I		Focus error input.
48	6	FDFCT	I		Connects a capacitor for time constant during defect.

Electrical Characteristics

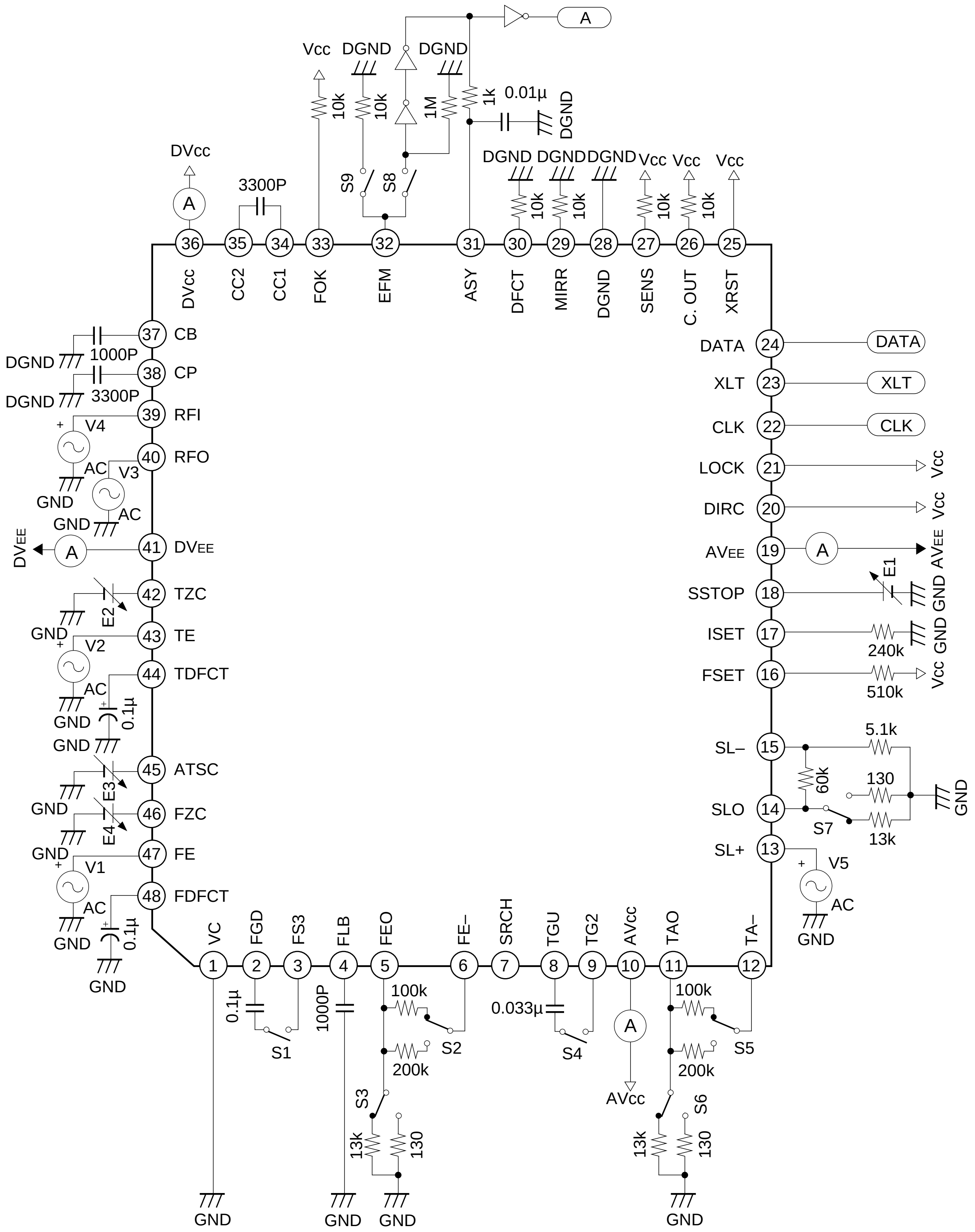
($Ta = 25°C$, $V_{CC} = 2.5V$, $V_{EE} = –2.5V$, D. GND = –2.5V)

No.		Item	Symbol	SW condition									SD	Bias condition				Measurement point	Description of output waveform and measurement method	Min.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9		E1	E2	E3	E4						
1		Current consumption	I_{CC}										00					10, 36		8	19	27	mA
2		Current consumption	I_{EE}										00					19, 41		–24	–17	–8	mA
3	FOCUS SERVO	DC voltage gain	G_{FEO}										08					5	V_1 = 10Hz, 100mVp-p G_{FEO} = 20 log (Vout/Vin)	18.0	21.0	24.0	dB
4	FOCUS SERVO	Feedthrough	V_{FEOF}										00					5	SG = 10kHz, 40mVp-p Difference in gain when SD = 00 and SD = 08			–35	dB
5	FOCUS SERVO	Max. output voltage	V_{FE01}		O								08					5	V_1 = 0.5V_{DC}	2.0			V
6	FOCUS SERVO	Max. output voltage	V_{FE02}		O								08					5	V_1 = –0.5V_{DC}			–2.0	V
7	FOCUS SERVO	Max. output voltage	V_{FE03}		O	O							08					5	V_1 = 0.5V_{DC}	1.2			V
8	FOCUS SERVO	Max. output voltage	V_{FE04}		O	O							08					5	V_1 = –0.5V_{DC}			–1.2	V
9	FOCUS SERVO	Search output voltage	V_{SRCH1}										02					5		–640		–360	mV
10	FOCUS SERVO	Search output voltage	V_{SRCH2}										03					5		360		640	mV
11	FOCUS SERVO	FZC threshold value	V_{FZC}										00				*	27	*(V_{CC} + DGND)/2 = SENS value when E4 is varied.	39	50	61	mV
12	TRACKING SERVO	DC voltage gain	G_{TEO}										25					11	V_2 = 10Hz, –500mVp-p G_{TEO} = 20 log (Vout/Vin)	11.6	13.3	17.6	dB
13	TRACKING SERVO	Feedthrough	V_{TEOF}										00					11	V_2 = 10kHz, 40mVp-p Difference in gain when SD = 00 and SD = 25			–39	dB
14	TRACKING SERVO	Max. output voltage	V_{TE01}					O					25					11	V_2 = –0.5V_{DC}	2.0			V
15	TRACKING SERVO	Max. output voltage	V_{TE02}					O					25					11	V_2 = 0.5V_{DC}			–2.0	V
16	TRACKING SERVO	Max. output voltage	V_{TE03}					O	O				25					11	V_2 = –0.5V_{DC}	1.2			V
17	TRACKING SERVO	Max. output voltage	V_{TE04}					O	O				25					11	V_2 = 0.5V_{DC}			–1.2	V
18	TRACKING SERVO	Jump output voltage	V_{JUMP1}										2C					11		–640		–360	mV
19	TRACKING SERVO	Jump output voltage	V_{JUMP2}										28					11		360		640	mV

No.		Item	Symbol	SW condition S1	S2	S3	S4	S5	S6	S7	S8	S9	SD	Bias condition E1	E2	E3	E4	Measurement point	Description of output waveform and measurement method	Min.	Typ.	Max.	Unit
20	TRACKING SERVO	ATSC threshold value	V_{ATSC1}										10			*		27	*(V_{CC} + DGND)/2 = SENS value when E3 is varied.	–45	–26	–7	mV
21	TRACKING SERVO	ATSC threshold value	V_{ATSC2}										10					27		7	26	45	mV
22	TRACKING SERVO	TZC threshold value	V_{TZC}										20		*			27	*(V_{CC} + DGND)/2 = SENS value when E2 is varied.	–20	0	20	mV
23	SLED SERVO	DC voltage gain	G_{SLO}										25					14	V_5 = 10Hz, 20mVp-p Open loop gain	50			dB
24	SLED SERVO	Feedthrough	V_{SLOF}										00					14	V_5 = 10kHz, 100mVp-p Difference in gain when SD = 00 and SD = 25			–34	dB
25	SLED SERVO	Max. output voltage	V_{SL01}										25					14	V_5 = 1.0V_{DC}	2.0			V
26	SLED SERVO	Max. output voltage	V_{SL02}										25					14	V_5 = –1.0V_{DC}			–2.0	V
27	SLED SERVO	Max. output voltage	V_{SL03}							O			25					14	V_5 = 1.0V_{DC}	2.0			V
28	SLED SERVO	Max. output voltage	V_{SL04}							O			25					14	V_5 = –1.0V_{DC}			–2.0	V
29	SLED SERVO	Kick output voltage	V_{KICK1}										23					14		–750		–450	mV
30	SLED SERVO	Kick output voltage	V_{KICK2}										22					14		450		750	mV
31	SLED SERVO	SSTOP threshold value	V_{SSTOP}										30	*				27	*(V_{CC} + DGND)/2 = SENS value when E1 is varied.	–40	–25	–10	mV
32		SENS Low level	V_{SENS}															27				–2.0	V
33		COUT Low level	V_{COUT}															26				–2.0	V
34	FOK	FOK threshold value	V_{FOKT}															33	(V_{CC} + DGND)/2 = value between Pins 39 and 40 when V_4 is varied.	–400	–356	–330	mV
35	FOK	High level voltage	V_{FOKH}															33	V_4 = 1Vp-p – 375mV_{DC}	2.2			V
36	FOK	Low level voltage	V_{FOKL}															33				–1.8	V
37	FOK	Max. operating frequency	F_{FOK}															33		45			kHz

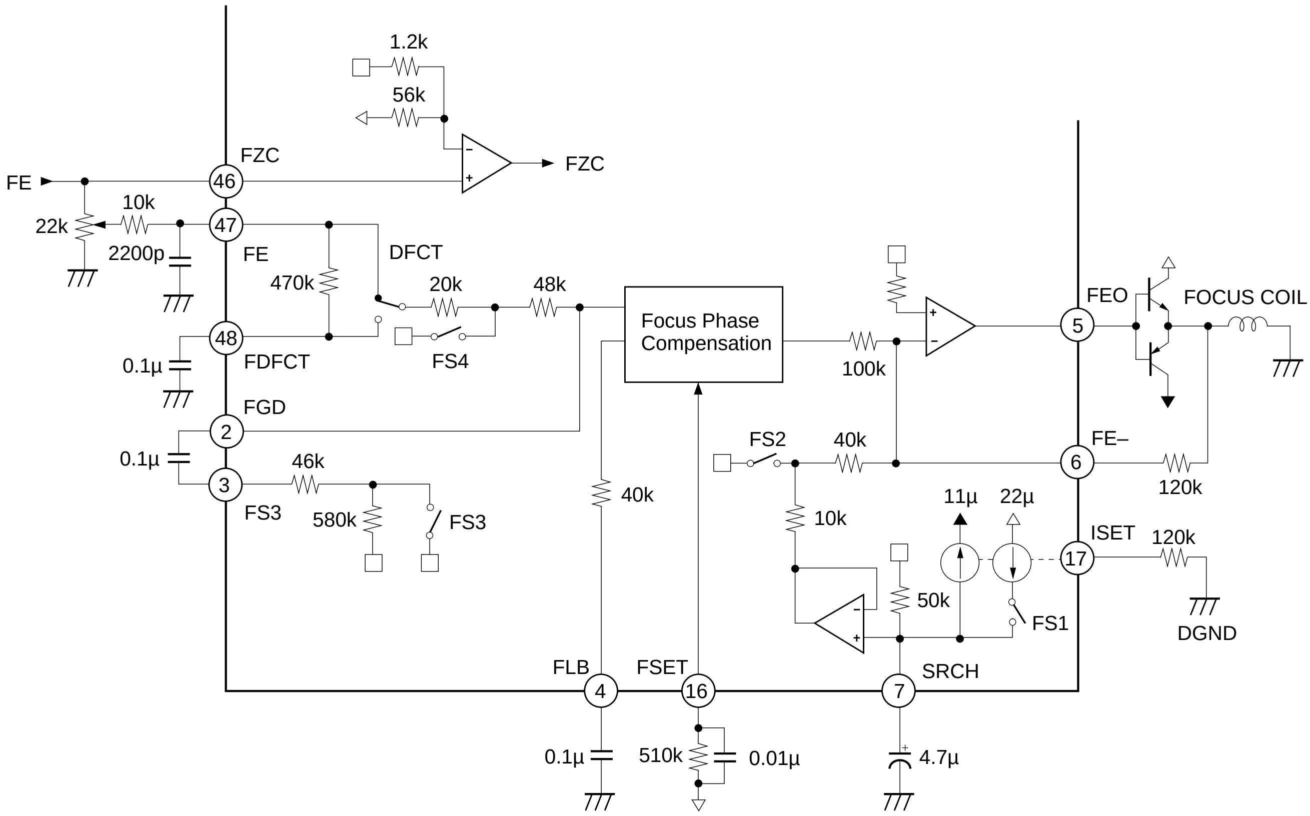
No.		Item	Symbol	SW condition									SD	Bias condition				Measure-ment point	Description of output waveform and measurement method	Min.	Typ.	Max.	Unit
				S1	S2	S3	S4	S5	S6	S7	S8	S9		E1	E2	E3	E4						
38	MIRROR	High level voltage	V_{MIRH}															29	V_4 = 10kHz 1.0Vp-p – 0.4V_{DC}	1.8			V
39		Low level voltage	V_{MIRL}															29				–2.0	V
40		Max. operating frequency	F_{MIR}															29	V_4 = 800mVp-p – 0.4V_{DC}	30			kHz
41		Min. input operating voltage	V_{MIR1}															29	V_4 = 10kHz – 0.4V_{DC}			0.3	Vp-p
42		Max. input operating voltage	V_{MIR2}															29		1.8			Vp-p
43	DEFECT	High level output voltage	V_{DFCTH}															30		1.8			V
44		Low level output voltage	V_{DFCTL}															30				–2.0	V
45		Min. operating frequency	F_{DFCT1}															30	V_4 = 0.8Vp-p + 375mV_{DC}			1	kHz
46		Max. operating frequency	F_{DFCT2}															30		2.5			kHz
47		Min. input operating voltage	V_{DFCT1}															30	V_4 = 50Hz + 375mV_{DC} (square wave)			0.5	Vp-p
48		Max. input operating voltage	V_{DFCT2}															30		1.8			Vp-p
49	EFM	Duty 1	D_{EFM1}								O							31	V_4 = 750kHz, 0.7Vp-p	–50	0	50	mV
50		Duty 2	D_{EFM2}								O							31	V_4 = 750kHz, 0.7Vp-p + 0.25V_{DC}	0	50	100	mV
51		High level output voltage	V_{EFMH}								O	O						32	V_4 = 750kHz, 0.7Vp-p	1.2			V
52		Low level output voltage	V_{EFML}								O	O						32				–1.2	V
53		Min. input operating voltage	V_{EFM1}								O							A	V_4 = 750kHz			0.12	Vp-p
54		Max. input operating voltage	V_{EFM2}								O							A		1.8			Vp-p

Electric Characteristics Measurement Circuit



Description of Functions

Focus Servo



The above figure shows a block diagram of the focus servo.

Ordinarily the FE signal is input to the focus phase compensation circuit through a 20kΩ and 48kΩ resistance; however, when DFCT is detected, the FE signal is switched to pass through a low-pass filter formed by the internal 470kΩ resistance and the capacitance connected to Pin 48. When this DFCT countermeasure circuit is not used, leave Pin 48 open.

When FS3 is ON, the high-frequency gain can be cut by forming a low-frequency time constant through a capacitor connected between Pins 2 and 3 and the internal resistor.

The capacitor connected between Pin 4 and GND is a time constant to boost the low frequency in the normal playback state.

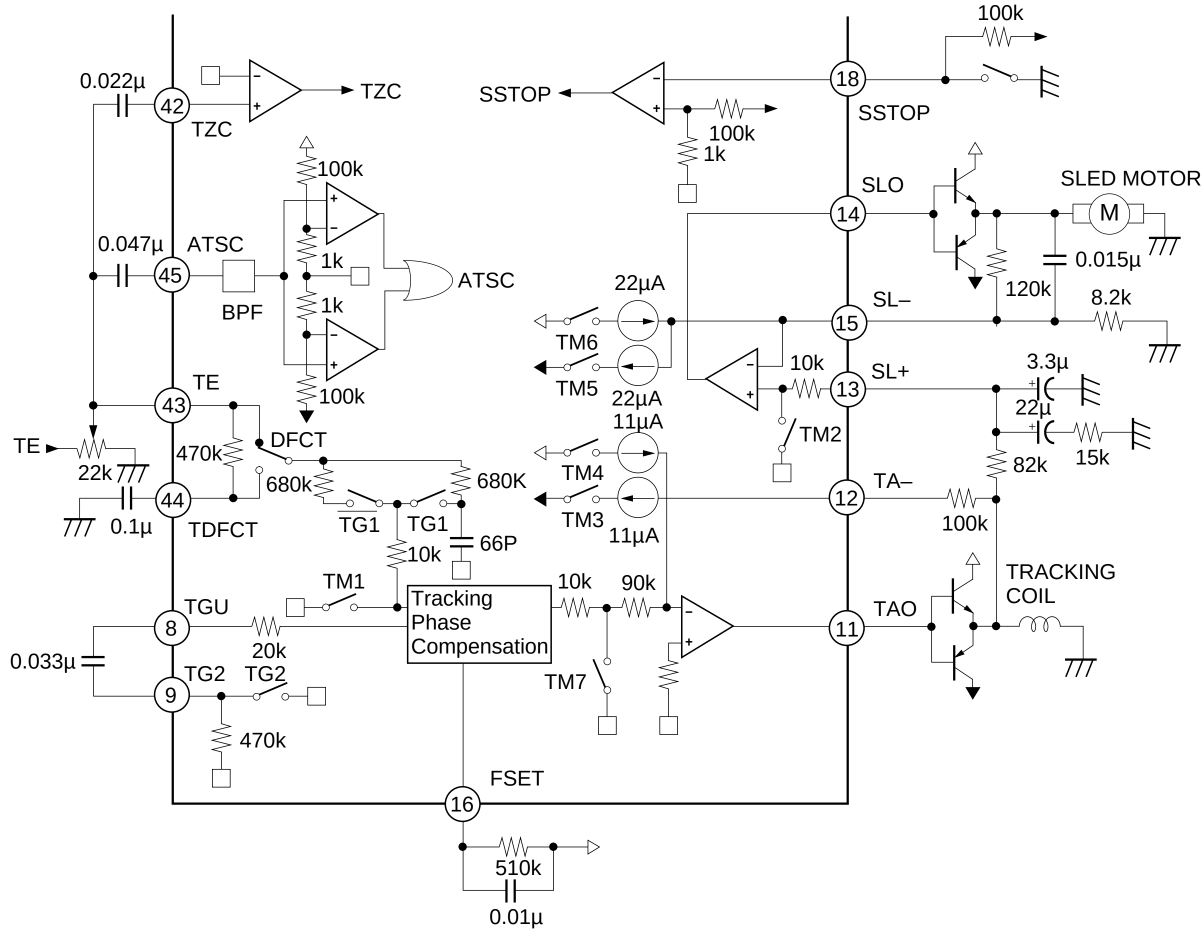
The peak frequency of the focus phase compensation is approximately 1.2kHz when a resistance of 510kΩ is connected to Pin 16.

The focus search level is approximately ±1.1Vp-p when using the constants indicated in the above figure. This level is inversely proportional to the resistance connected between Pin 17 and GND. However, changing this resistance also changes the level of the track jump and sled kick as well.

The FZC comparator inverted input is set to 2% of V_{CC} and VC (Pin 1); $(V_{CC} - VC) \times 2\%$.

* 510kΩ resistance is recommended for Pin 16.

Tracking Sled Servo



The above figure shows a block diagram of the tracking and sled servo.

The capacitor connected between Pins 8 and 9 is a time constant to cut the high-frequency gain when TG2 is OFF. The peak frequency of the tracking phase compensation is approximately 1.2kHz when a 510kΩ resistance connected to Pin 16.

To jump tracks in FWD and REV directions, turn TM3 or TM4 ON. During this time, the peak voltage applied to the tracking coil is determined by the TM3 or TM4 current and the feedback resistance from Pin 12. To be more specific,

Track jump peak voltage = TM3 (or TM4) current × feedback resistance

The FWD and REV sled kick is performed by turning TM5 or TM6 ON. During this time, the peak voltage applied to the sled motor is determined by the TM5 or TM6 current and the feedback resistance from Pin 15;

Sled kick peak voltage = TM5 (or TM6) current × feedback resistance

The values of the current for each switch are determined by the resistance connected between Pin 17 and GND. When this resistance is 120kΩ:

TM3 (or TM4) = ±11µA, and TM5 (or TM6) = ±22µA.

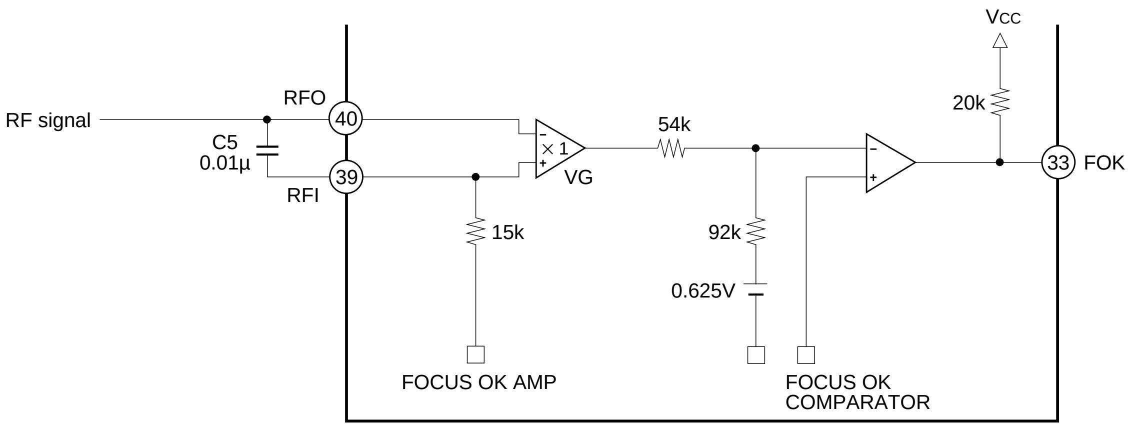
This current value is almost inversely proportional to the resistance and the variable range is approximately 5 to 40µA at TM3.

SSTOP is the ON/OFF detection signal for the limit SW of the linear motor's innermost track.

As is the case with the FE signal, the TE signal is switched to pass through a low-pass filter formed by the internal resistance (470kΩ) and the capacitor connected to Pin 44.

TM-1 was ON at DFCT in the CXA1082 and CXA1182, but it does not operate in the CXA1372.

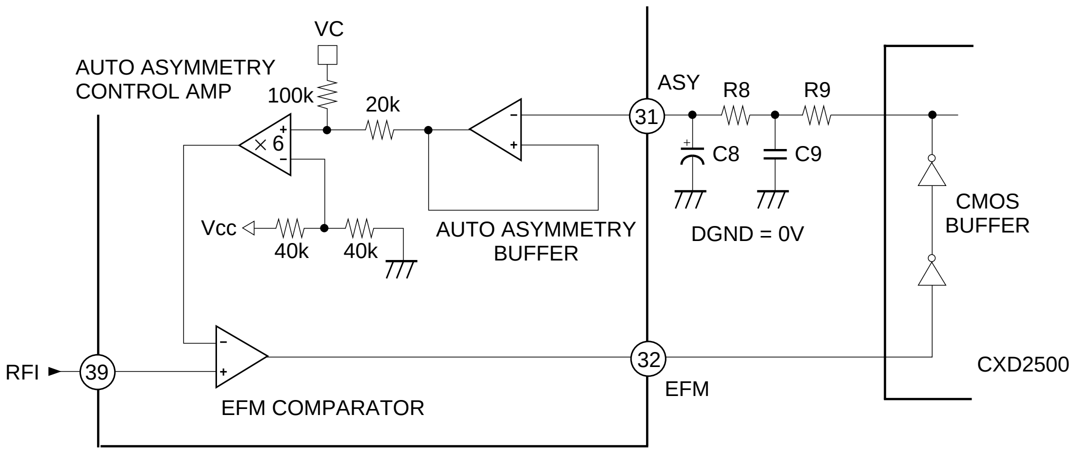
Focus OK circuit



The focus OK circuit creates the timing window okaying the focus servo from the focus search state.
The HPF output is obtained at Pin 39 from Pin 40 (RF signal), and the LPF output (opposite phase) of the focus OK amplifier output is also obtained.
The focus OK output reverses when $V_{RFI} – V_{RFO} \approx –0.37V$.
Note that, C5 determines the time constants of the HPF for the EFM comparator and mirror circuit and the LPF of the focus OK amplifier. Ordinarily, with a C5 equal to 0.01μF selected, the fc is equal to 1kHz, and block error rate degradation brought about by RF envelope defects caused by scratched discs can be prevented.

EFM comparator

EFM comparator changes RF signal to a binary value. The asymmetry generated due to variations in disc manufacturing cannot be eliminated by the AC coupling alone. Therefore, the reference voltage of EFM comparator is controlled through 1 and 0 that are in approximately equal numbers in the binary EFM signals.



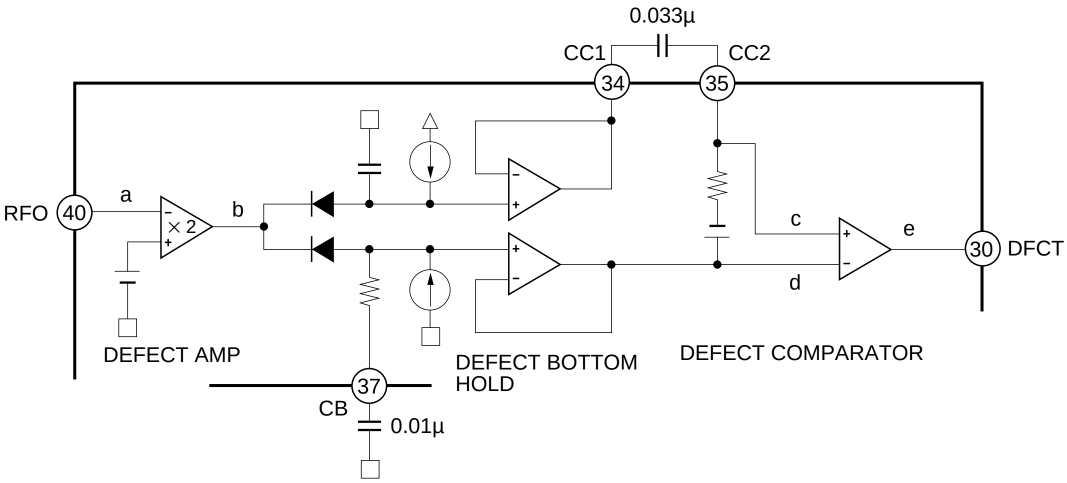
As this comparator is a current SW type, each of the High and Low levels is not equal to the power supply voltage. A feedback has to be applied through the CMOS buffer.
R8, R9, C8, and C9 form a LPF to obtain (V_{CC} + DGND)/2V. When fc (cut-off frequency) exceeds 500Hz, the EFM low-frequency components leak badly, and the block error rate worsens.

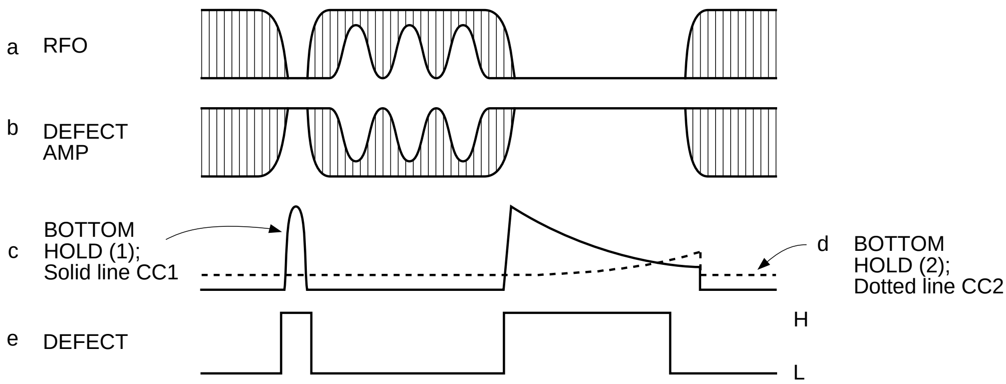
DEFECT circuit

After inversion, RFI signal is bottom held by means of the long and short time constants. The long time-constant bottom hold keeps the mirror level prior to the defect.

The short time-constant bottom hold responds to a disc mirror defect in excess of 0.1ms, and this is differentiated and level-shifted through the AC coupling circuit.

The long and short time-constant signals are compared to generate at mirror defect detection signal.

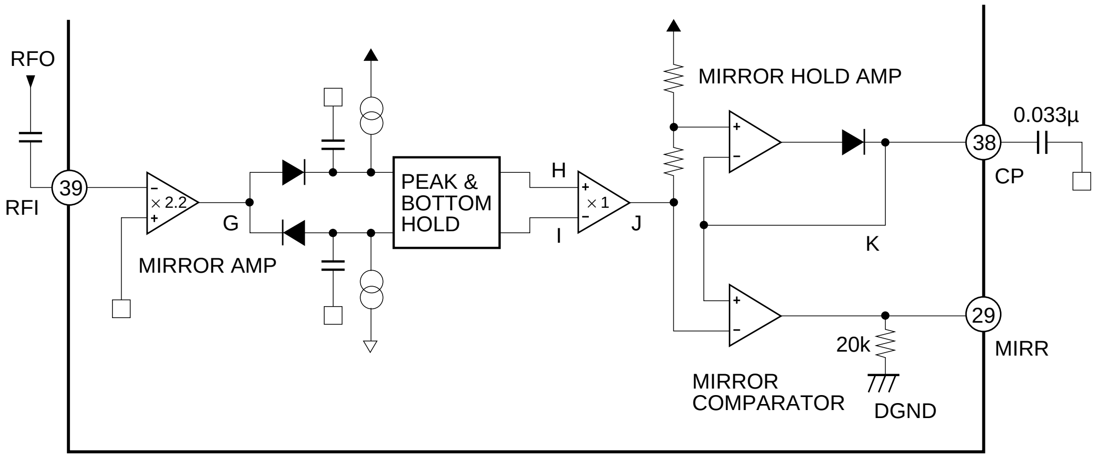


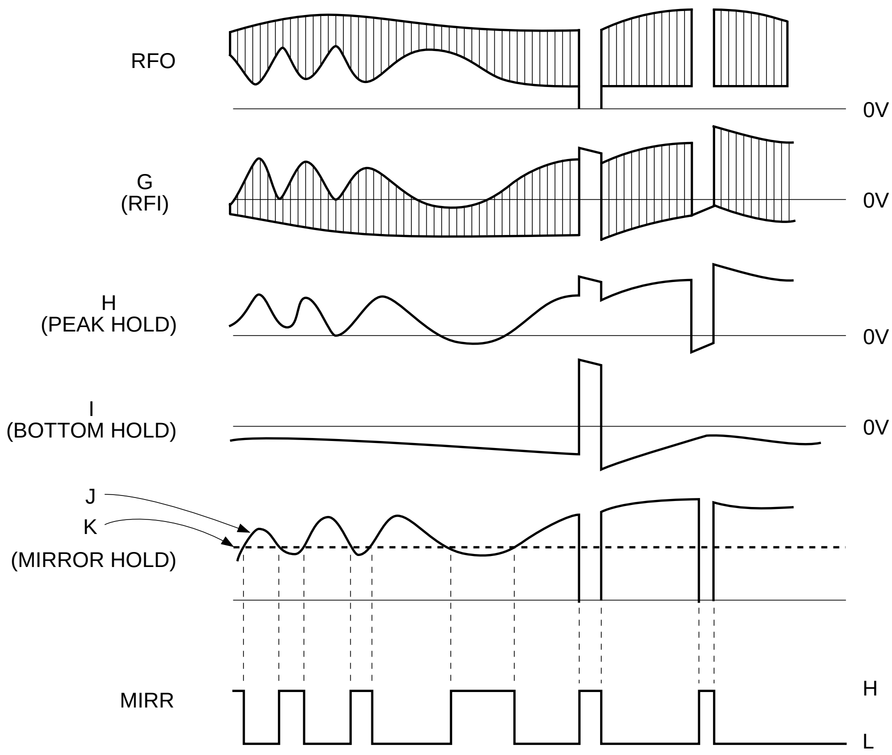


Mirror Circuit

The mirror circuit performs peak and bottom hold after the RFI signal has been amplified.

For the peak hold, a time constant can follow a 30kHz traverse, and, for the bottom hold, one can follow the rotation cycle envelope fluctuation.





Through differential amplification of the peak and bottom hold signals H and I, mirror output can be obtained by comparing an envelope signal J (demodulated to DC) to signal K for Which peak holding at a level 2/3 that of the maximum was performed with a large time constant. In other words, mirror output is low for tracks on the disc and high for the area between tracks (the MIRR areas). In addition, a high signal is output when a defect is detected. The mirror hold time constant must be sufficiently large in comparison with the traverse signal.

Commands

The input data to operate this IC is configured as 8-bit data; however, below, this input data is represented by 2-digit hexadecimal numerals in the form $XX, where X is a hexadecimal numeral between 0 and F.
Commands for the CXA1372 can be broadly divided into four groups ranging in value from $0X to $3X.

1. $0X (“FZC” at SENS (Pin 27))

These commands are related to focus servo control.
The bit configuration is as shown below.

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	FS4	FS3	FS2	FS1

Four focus-servo related switches exist: FS1 to FS4 corresponding to D0 to D3, respectively.

$00 When FS1 = 0, Pin 7 is charged to $(22\mu A - 11\mu A) \times 50k\Omega = 0.55V$.
If FS2 = 0, this voltage is no longer transferred, and the output at Pin 5 becomes 0V.

$02 From the state described above, the only FS2 becomes 1. When this occurs, a negative signal is output to Pin 5. This voltage level is obtained by equation 1 below.

$$(22\mu A - 11\mu A) \times 50k\Omega \times \frac{\text{resistance between Pins 5 and 6}}{50k\Omega} \quad \cdots\cdots \quad \text{Equation 1}$$

$03 From the state described above, FS1 becomes 1, and a current source of +22µA is split off.
Then, a CR charge/discharge circuit is formed, and the voltage at Pin 7 decreases with the time as shown in Fig. 1 below.

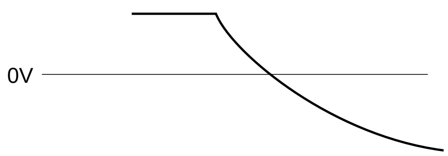


Fig. 1. Voltage at Pin 7 when FS1 gose from 0 → 1

This time constant is obtained with the 50kΩ resistance and an external capacitor.

By alternating the commands between $02 and $03, the focus search voltage can be constructed. (Fig. 2)

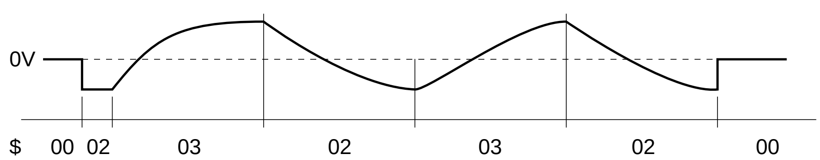


Fig. 2. Constructing the search voltage by alternating between $02 and $03 (Voltage at Pin 5)

1-1. FS4

This switch is provided between the focus error input (Pin 47) and the focus phase compensation, and is in charge of turning the focus servo ON and OFF.

$00 → $08
Focus OFF ← Focus ON

1-2. Procedure of focus activation

For description, suppose that the polarity is as described below.
a) The lens is searching the disc from far to near;
b) The output voltage (Pin 5) is changing from negative to positive; and
c) The focus S-curve is varying as shown below.

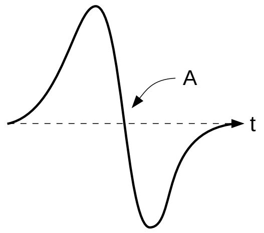


Fig. 3. S-curve

The focus servo is activated at the operating point indicated by A in Fig. 3. Ordinarily, focus searching and turning the focus servo switch ON are performed when the focus S-curve transits the point A indicated in Fig. 3. To prevent misoperation, this signal is ANDed with the focus OK signal.
In this IC, FZC (Focus Zero Cross) signal is output from the SENS pin (Pin 27) as the point A transit signal. Focus OK is output as a signal indicating that the signal is in focus (can be in focus in this case).
Following the line of the above description, focusing can be well obtained by observing the following timing chart.

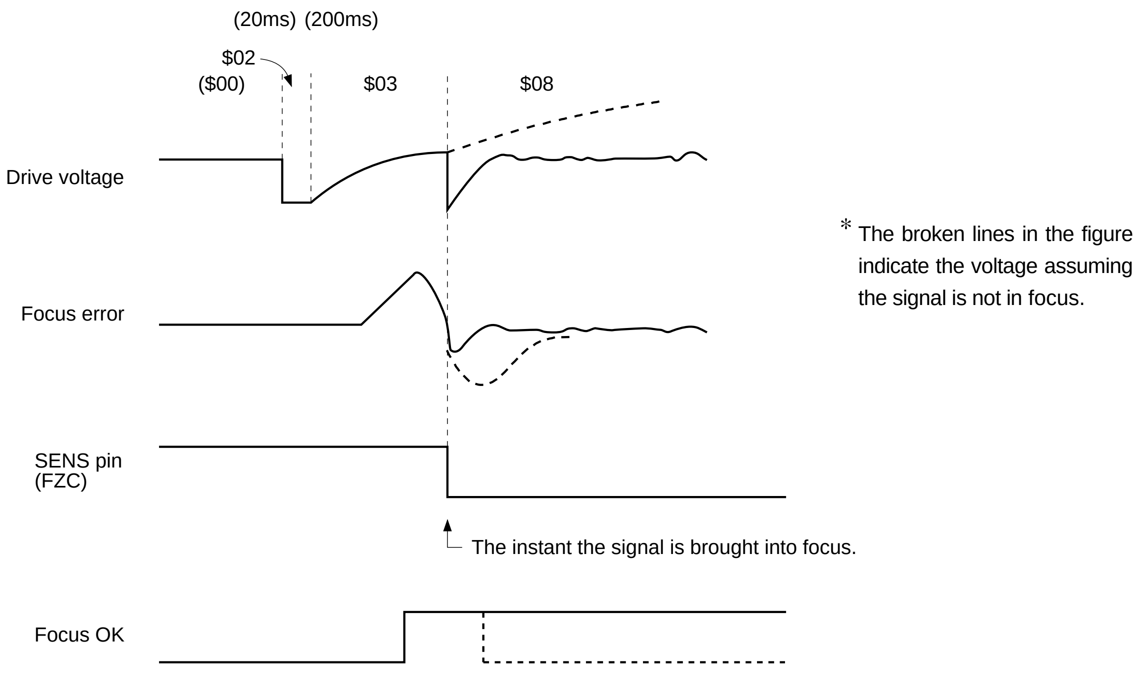


Fig. 4. Focus ON timing chart

Note that the time from the High to Low transition of FZC to the time command $08 is asserted must be minimized. To do this, the software sequence shown in B is better than the sequence shown in A.

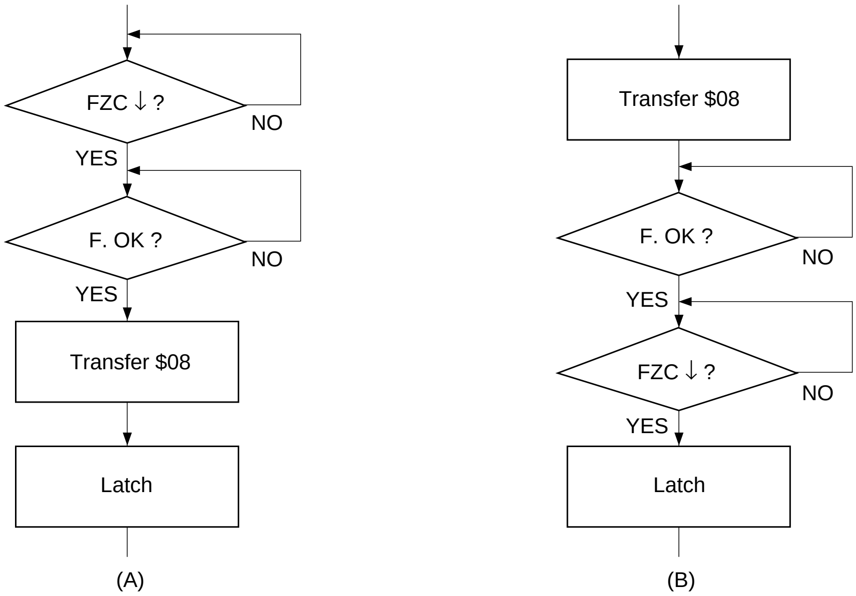


Fig. 5. Poor and good software command sequences

1-3. SENS (Pin 27)

The output of the SENS pin differs depending on the input data as shown below.

$0X: FZC
$1X: AS
$2X: TZC
$3X: SSTOP
$4X to 7X: HIGH-Z

2. $1X ("AS" at SENS (Pin 27))

These commands deal with switching TG1 and TG2 ON/OFF.
The bit configuration is as follows

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	ANTI SHOCK ON/OFF	Break circuit ON/OFF	TG2	TG1

TG1, TG2

The purpose of these switches is to switch the tracking servo gain Up/Normal. The brake circuit (TM7) is to prevent the frequently occurred phenomena where the merely 10-track jump has been performed actually though a 100-track jump was intended to be done due to the extremely degraded actuator settling caused by the servo motor exceeding the linear range after a 100 or 10-track jump.

When the actuator travels radially; that is, when it traverses from the inner track to the outer track of the disc and vice versa, the brake circuit utilizes the fact that the phase relationship between the RF envelope and the tracking error is 180°out-of-phase to cut the unneeded portion of the tracking error and apply braking.

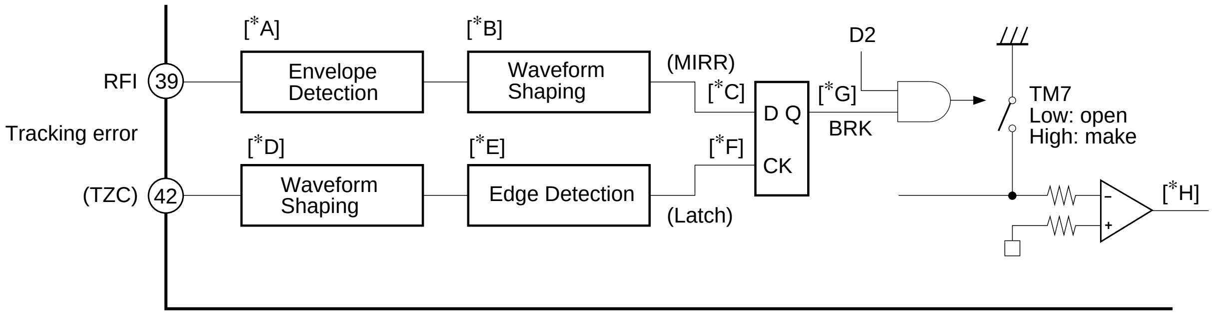


Fig. 6. TM7 operation (brake circuit)

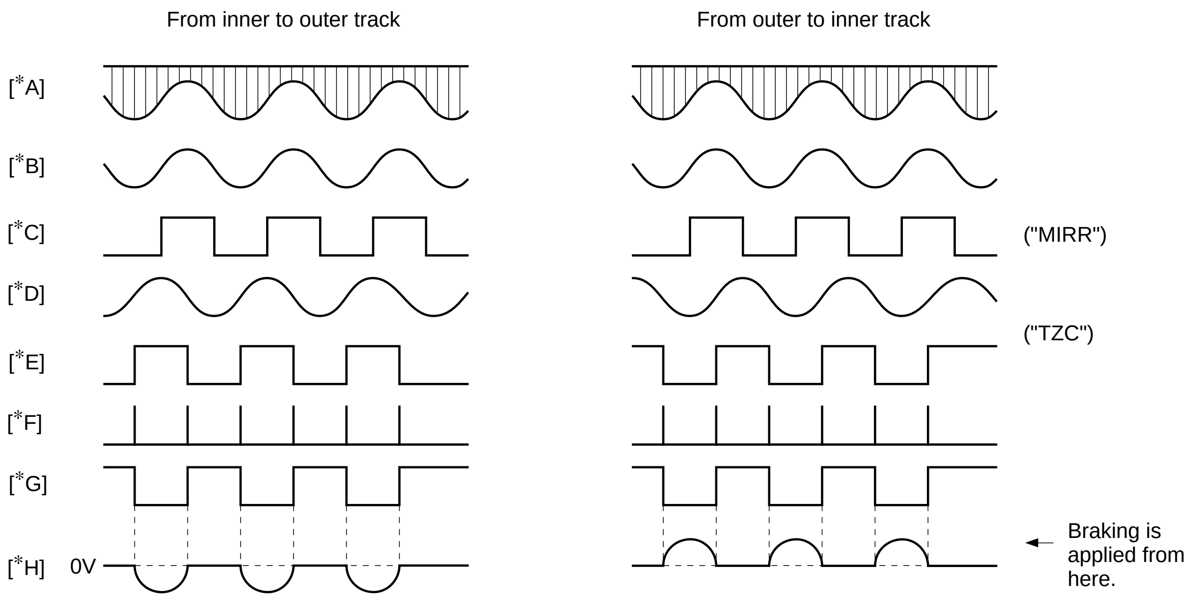


Fig. 7. Internal waveform

3. $2X (“TZC” at SENS (Pin 27))

These commands deal with turning the tracking servo and sled servo ON/OFF, and creating the jump pulse and fast forward pulse during access operations.

D7	D6	D5	D4	D3 D2	D1 D0
0	0	1	0	Tracking control 00: OFF 01: Servo ON 10: F-JUMP 11: R-JUMP ↓ TM1, TM3, TM4	Sled control 00: OFF 01: Servo ON 10: F-FAST FORWARD 11: R-FAST FORWARD ↓ TM2, TM5, TM6

DIRC (Pin 20) and 1 Track Jump

Normally, an acceleration pulse is applied for a 1-track jump. Then a deceleration pulse is given for a specified time observing the tracking error from the moment it passes point 0, and tracking servo is turned ON again. For the 100-track jump to be explained in the next item, as long as the number of tracks is about 100 there is no problem. However a 1-track jump must be performed here, which requires the above complicated procedure. For the 1-track jump in CD players, both the acceleration and deceleration take about 300 to 400µs. When software is used to execute this operation, it turns out as shown in the flow chart of Fig. 9. Actually, it takes some time to transfer data.

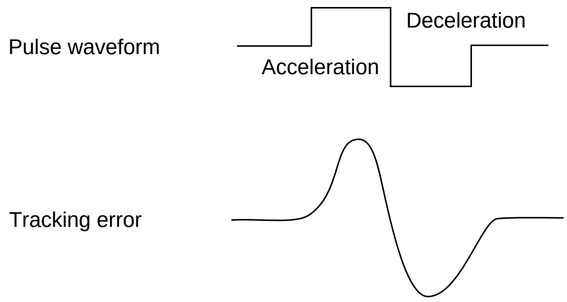


Fig. 8. Pulse waveform and tracking error of 1-track jump

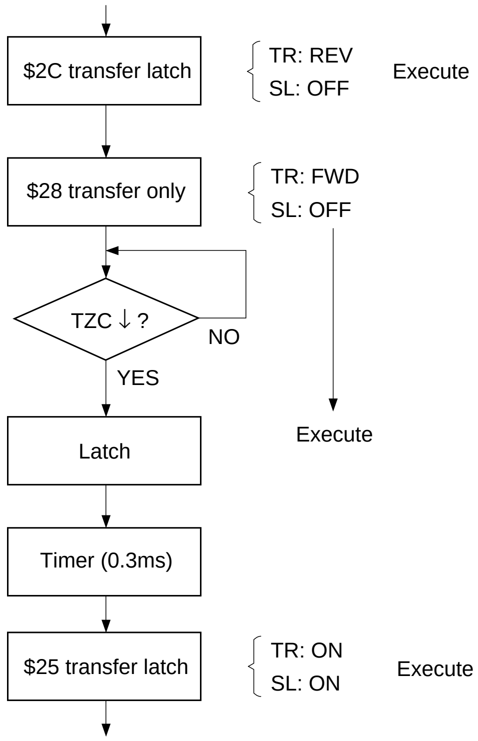


Fig. 9. 1-track jump not using DIRC (Pin 20)

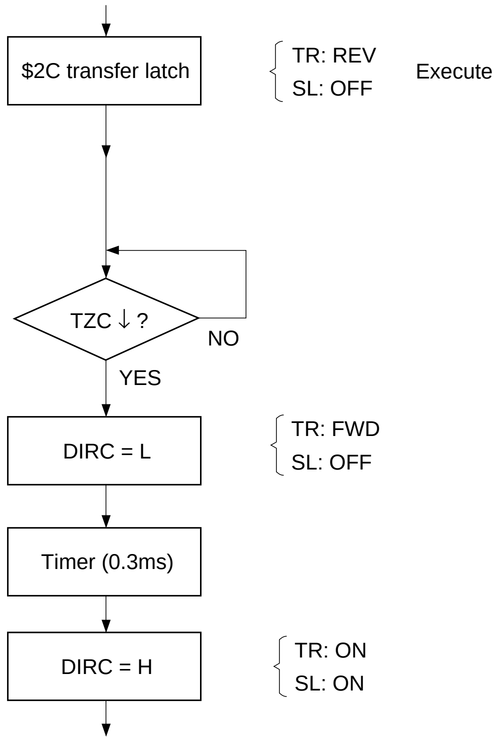


Fig. 10. 1-track jump with DIRC (Pin 20)

The DIRC (Direct Control) pin was provided in this IC to facilitate the 1-track jump operation. Conduct the following process to perform 1-track jump using DIRC (normal High).

(a) Acceleration pulse is output. ($2C for REV or $28 for FWD).

(b) With TZC ↓ (or TZC ↑), set DIRC to Low. (SENS Pin 27 outputs "TZC"). As the jump pulse polarity is inverted, deceleration is applied.

(c) Set DIRC to High after a specific time.
Both the tracking servo and sled servo are switched ON automatically.
As a result, the track jump turns out as shown in the flow chart of Fig. 10 and the two serial data transfers can be omitted.

4. $3X

This command selects the focus search and sled kick levels.

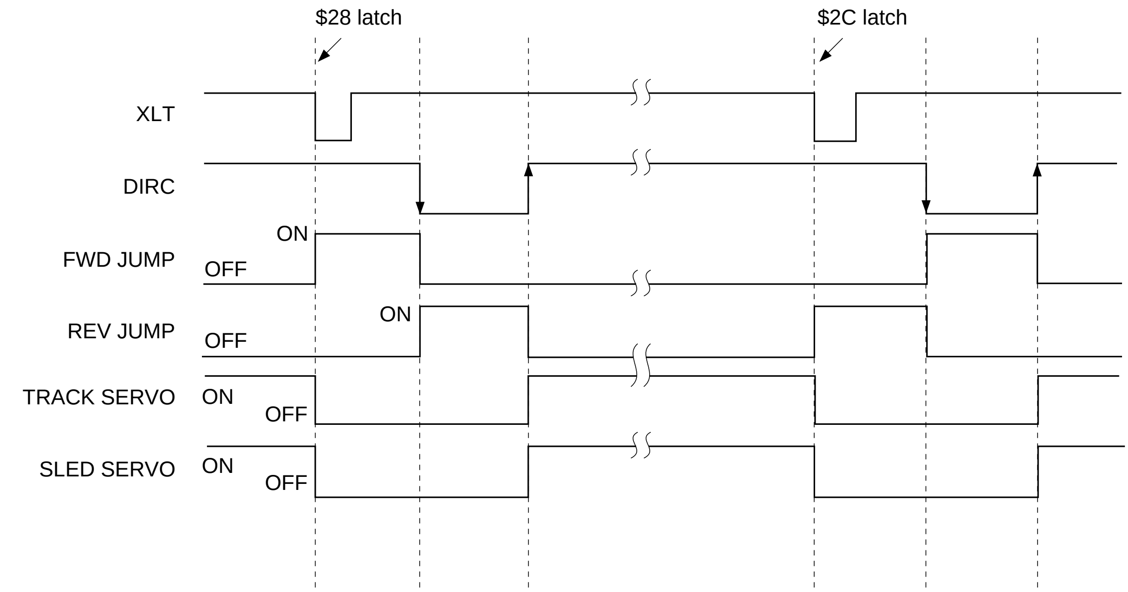
D0, D1 ..... Sled, NORMAL feed, high-speed feed

D2, D3 ..... Focus search level selection

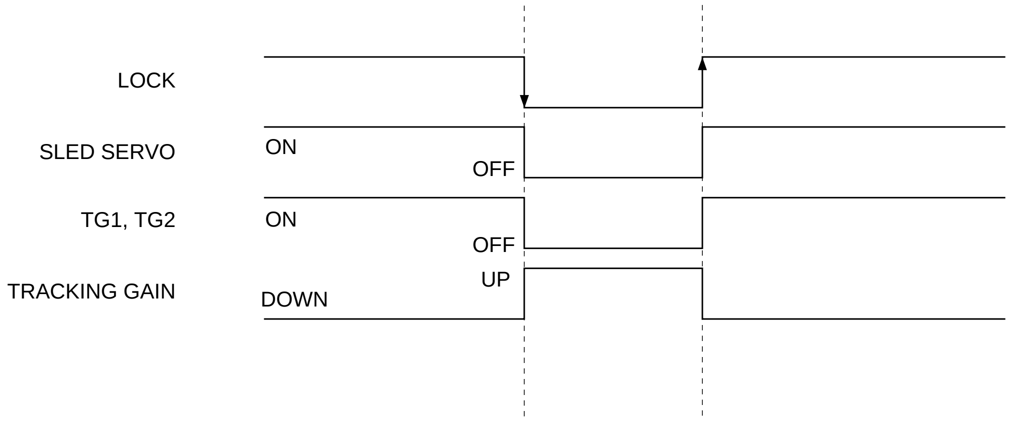
D7 D6 D5 D4	Focus search level		Sled kick level		Relative value
	D3 (PS4)	D2 (PS3)	D1 (PS2)	D0 (PS1)	
0 0 1 1	0	0	0	0	±1
	0	1	0	1	±2
	1	0	1	0	±3
	1	1	1	1	±4

Parallel Direct Interface

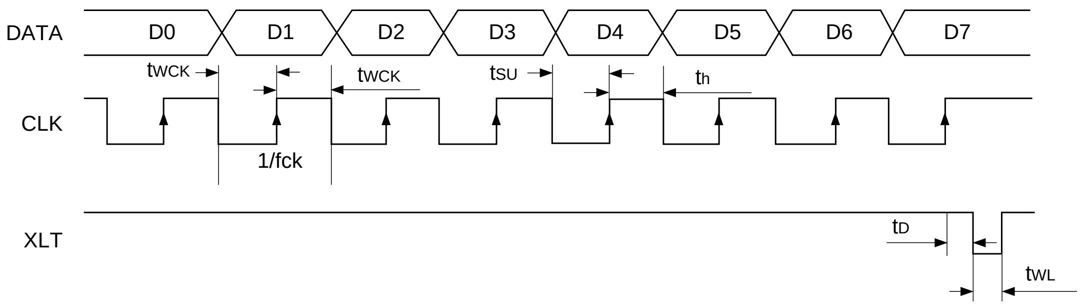
1. DIRC



2. LOCK (Sled overrun prevention circuit)



CPU Serial Interface Timing Chart



(DVcc – DGND = 4.5 to 5.5V)

Item	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	fck			1	MHz
Clock pulse width	fwck	500			ns
Setup time	tsu	500			ns
Hold time	th	500			ns
Delay time	tD	1000			ns
Latch pulse width	tWL	1000			ns

System Control

Item	Address	Data				SENS output
	D7 D6 D5 D4	D3	D2	D1	D0	
Focus control	0 0 0 0	FS4 Focus ON	FS3 Gain Down	FS2 Search ON	FS1 Search Up	FZC
Tracking control	0 0 0 1	Anti-shock	Brake ON	TG2 Gain set *1	TG1	A. S
Tracking mode	0 0 1 0	Tracking mode *2		Sled mode *3		TZC
Select	0 0 1 1	PS4 Focus search + 2	PS3 Focus search + 1	PS2 Sled kick + 2	PS1 Sled kick + 1	SSTOP

*1 Gain set
TG1 and TG2 can be set independently.
When the anti-shock is at 1 (00011xxx), both TG1 and TG2 are inverted when the internal anti-shock is at High.

*2 Tracking mode

	D3	D2
OFF	0	0
ON	0	1
FWD JUMP	1	0
REV JUMP	1	1

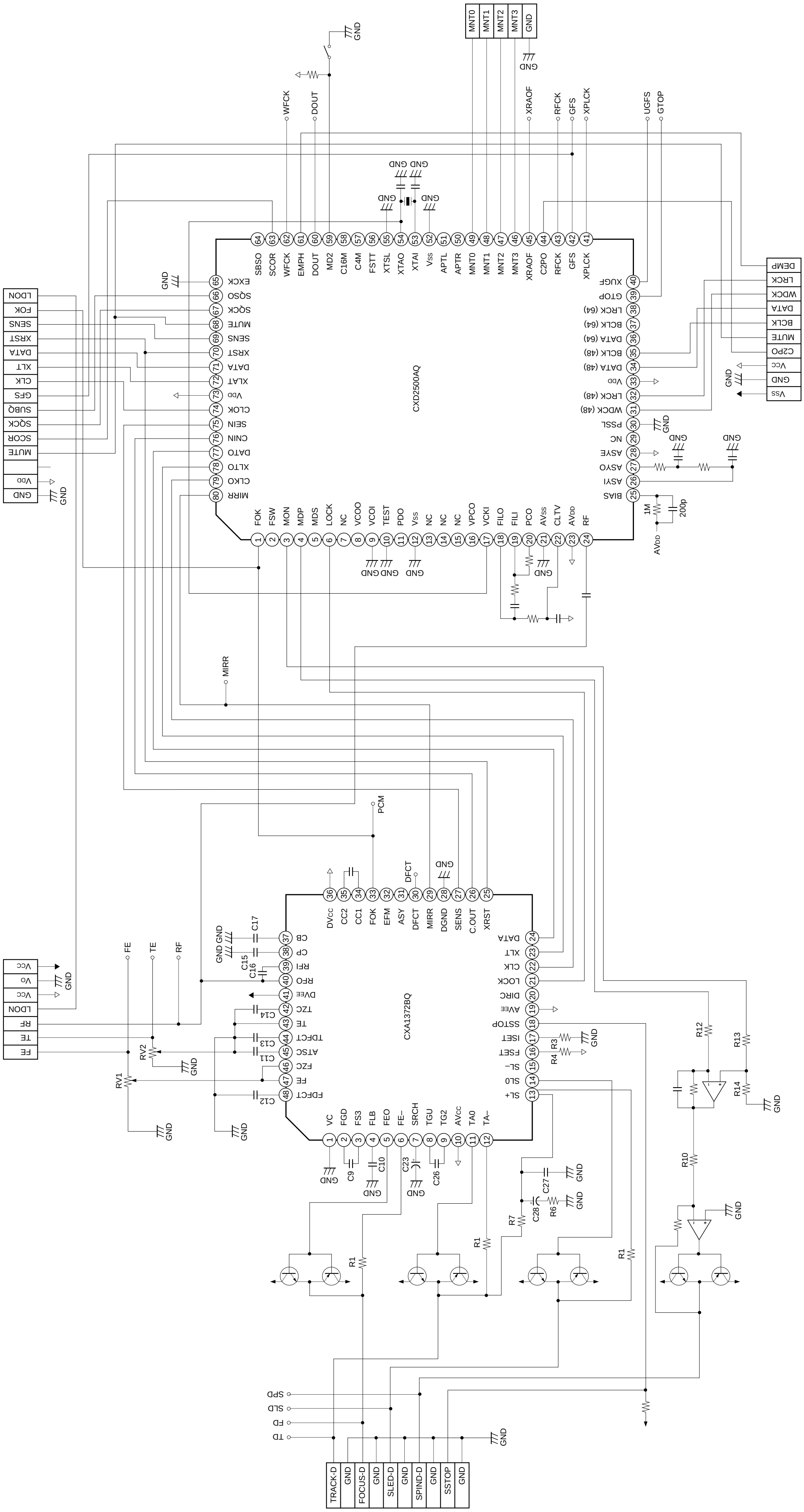
*3 Sled mode

	D1	D0
OFF	0	0
ON	0	1
FWD MOVE	1	0
REV MOVE	1	1

Serial Data Truth Table

Serial data	Hex.	Function		
FOCUS CONTROL		FS = 4 3 2 1		
0 0 0 0 0 0 0 0	$00	0 0 0 0		
0 0 0 0 0 0 0 1	$01	0 0 0 1		
0 0 0 0 0 0 1 0	$02	0 0 1 0		
0 0 0 0 0 0 1 1	$03	0 0 1 1		
0 0 0 0 0 1 0 0	$04	0 1 0 0		
0 0 0 0 0 1 0 1	$05	0 1 0 1		
0 0 0 0 0 1 1 0	$06	0 1 1 0		
0 0 0 0 0 1 1 1	$07	0 1 1 1		
0 0 0 0 1 0 0 0	$08	1 0 0 0		
0 0 0 0 1 0 0 1	$09	1 0 0 1		
0 0 0 0 1 0 1 0	$0A	1 0 1 0		
0 0 0 0 1 0 1 1	$0B	1 0 1 1		
0 0 0 0 1 1 0 0	$0C	1 1 0 0		
0 0 0 0 1 1 0 1	$0D	1 1 0 1		
0 0 0 0 1 1 1 0	$0E	1 1 1 0		
0 0 0 0 1 1 1 1	$0F	1 1 1 1		
TRACKING CONTROL		AS = 0	AS = 1	
		TG = 2 1	TG = 2 1	
0 0 0 1 0 0 0 0	$10	0 0	0 0	
0 0 0 1 0 0 0 1	$11	0 1	0 1	
0 0 0 1 0 0 1 0	$12	1 0	1 0	
0 0 0 1 0 0 1 1	$13	1 1	1 1	
0 0 0 1 0 1 0 0	$14	0 0	0 0	
0 0 0 1 0 1 0 1	$15	0 1	0 1	
0 0 0 1 0 1 1 0	$16	1 0	1 0	
0 0 0 1 0 1 1 1	$17	1 1	1 1	
0 0 0 1 1 0 0 0	$18	0 0	1 1	
0 0 0 1 1 0 0 1	$19	0 1	1 0	
0 0 0 1 1 0 1 0	$1A	1 0	0 1	
0 0 0 1 1 0 1 1	$1B	1 1	0 0	
0 0 0 1 1 1 0 0	$1C	0 0	1 1	
0 0 0 1 1 1 0 1	$1D	0 1	1 0	
0 0 0 1 1 1 1 0	$1E	1 0	0 0	
0 0 0 1 1 1 1 1	$1F	1 1	0 1	
TRACKING MODE		DIRC = 1 TM = 654321	DIRC = 0 654321	DIRC = 1 654321
0 0 1 0 0 0 0 0	$20	000000	001000	000011
0 0 1 0 0 0 0 1	$21	000010	001010	000011
0 0 1 0 0 0 1 0	$22	010000	011000	100001
0 0 1 0 0 0 1 1	$23	100000	101000	100001
0 0 1 0 0 1 0 0	$24	000001	000100	000011
0 0 1 0 0 1 0 1	$25	000011	000110	000011
0 0 1 0 0 1 1 0	$26	010001	010100	100001
0 0 1 0 0 1 1 1	$27	100001	100100	100001
0 0 1 0 1 0 0 0	$28	000100	001000	000011
0 0 1 0 1 0 0 1	$29	000110	001010	000011
0 0 1 0 1 0 1 0	$2A	010100	011000	100001
0 0 1 0 1 0 1 1	$2B	100100	101000	100001
0 0 1 0 1 1 0 0	$2C	001000	000100	000011
0 0 1 0 1 1 0 1	$2D	001010	000110	000011
0 0 1 0 1 1 1 0	$2E	011000	010100	100001
0 0 1 0 1 1 1 1	$2F	101000	100100	100001

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Notes on Operation

1. Connection of the power supply pin

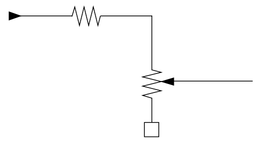
	Vcc	V_{EE}	VC
dual ±5V power supplies	+5V	–5V	0V
single 5V power supplies	+5V	0V	VC

2. FSET pin
The FSET pin determines the cut-off frequency fc for the focus and tracking high-frequency phase compensation.

3. ISET pin
ISET current = 1.27V/R
= Focus search current
= Tracking jump current
= 1/2 sled kick current

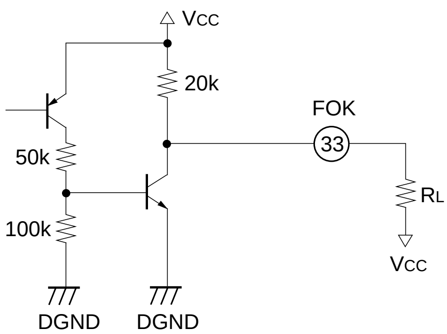
4. The tracking amplifier input is clamped at $1V_{BE}$ to prevent overinput.

5. FE (focus error) and TE (tracking error) gain changing method
(1) High gain: Resistance between FE pins (Pins 5 and 6) 100kΩ → Large
Resistance between TA pins (Pins 11 and 12) 100kΩ → Large
(2) Low gain: A signal, whose resistance is divided, is input to FE and TE.



6. Input voltage of microcomputer interface Pins 20 to 25, should be set as follows.
V_{IH} $V_{CC} \times$ 90% or more
V_{IL} $V_{CC} \times$ 10% or less

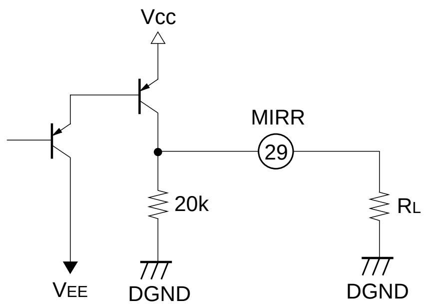
7. Focus OK circuit
(1) Refer to the "Description of Operation" for the time constant setting of the focus OK amplifier LPF and the mirror amplifier HPF.
(2) The equivalent circuit of FOK output pin is as follows.



FOK comparator output is:
Output voltage High: V_{FOKH} ≈ near Vcc
Output voltage Low: V_{FOKL} ≈ Vsat (NPN) + DGND

8. Mirror Circuit

(1) The equivalent circuit of MIRR output pin is as follows.



MIRR comparator output is:

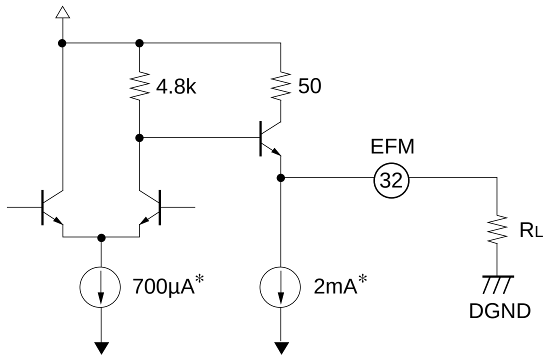
Output voltage High: $V_{MIRH} \approx V_{CC}$ – Vsat (LPNP)

Output voltage Low: $V_{MIRL} \approx$ near DGND

9. EFM Comparator

(1) Note that EFM duty varies when the CXA1372 Vcc differs from that of DSP IC (such as the CXD2500).

(2) The equivalent circuit of the EFM output pin is as follows.



* When the power supply current between Vcc and DGND is 5V.

EFM comparator output is:

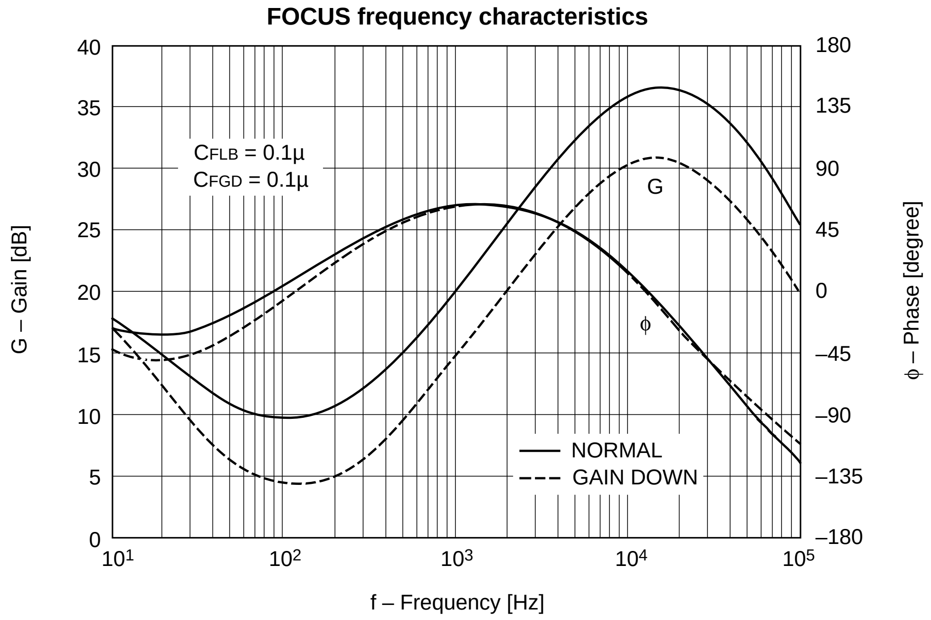
Output voltage High: $V_{EFMH} \approx V_{CC} - V_{BE}$ (NPN)

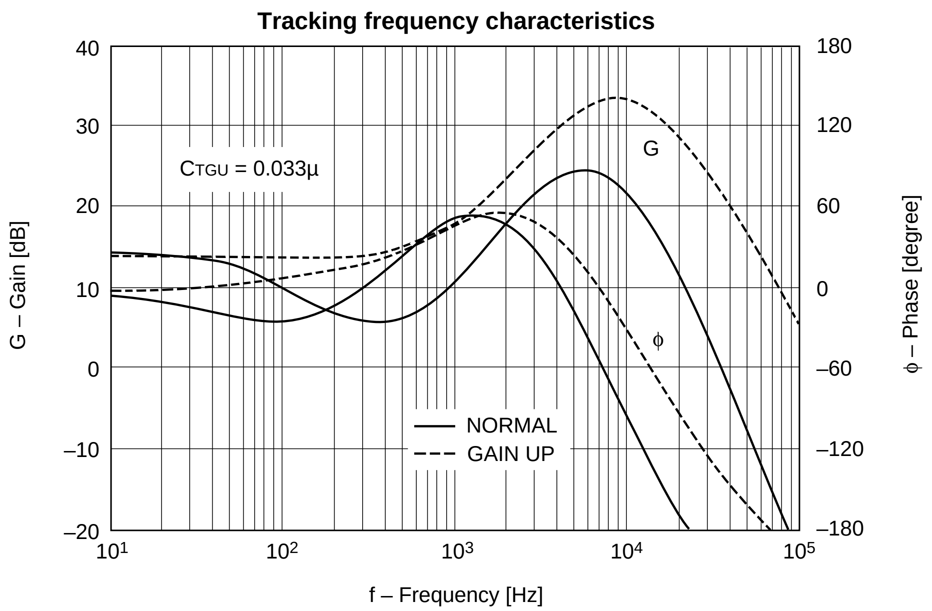
Output voltage Low: $V_{EFML} \approx V_{CC} - 4.8\ (k\Omega) \times 700\ (\mu A) - V_{BE}$ (NPN)

Standard Circuit Design Data for Focus/Tracking Internal Phase Compensation

Mode	Item	Symbol	SW condition									SD	Bias condition				Measure-ment point	Description of output waveform and measurement method	Min.	Typ.	Max.	Unit
			S1	S2	S3	S4	S5	S6	S7	S8	S9		E1	E2	E3	E4						
FOCUS	1.2kHz gain		O									08					5	When C_{FLB} = 0.1μF		21.5		dB
	1.2kHz phase		O									08					5			63		deg
	1.2kHz gain		O									0C					5			16		dB
	1.2kHz phase		O									0C					5			63		deg
TRACKING	1.2kHz gain					O						25					11			13		dB
	1.2kHz phase					O						25					11			–125		deg
	2.7kHz gain					O						25 13					11			26.5		dB
	2.7kHz phase					O						25 13					11			–130		deg

Example of Representative Characteristics

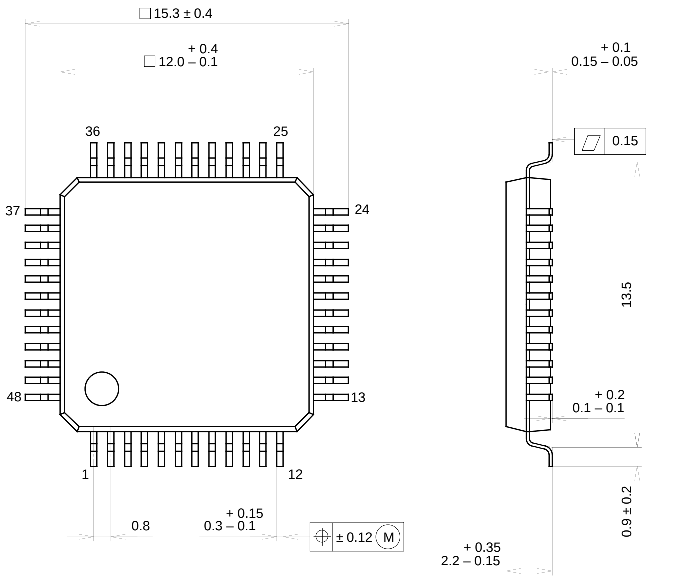




Package Outline Unit: mm

CXA1372BQ

48PIN QFP (PLASTIC)



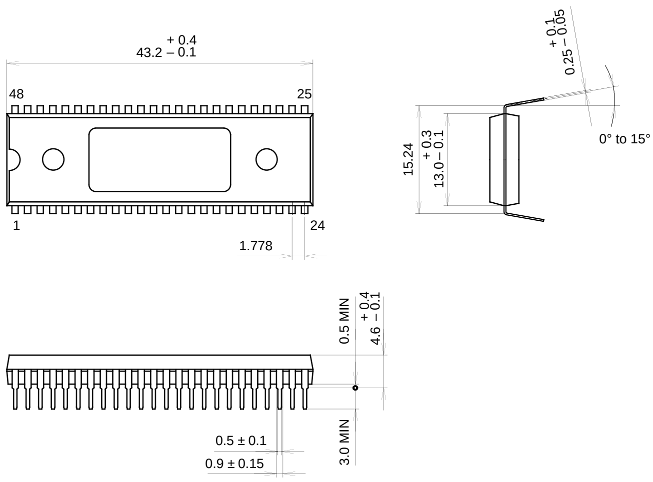
PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	———

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

CXA1372BS

48PIN SDIP (PLASTIC) 600mil



PACKAGE STRUCTURE

SONY CODE	SDIP-48P-02
EIAJ CODE	SDIP048-P-0600-A
JEDEC CODE	———

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	5.1g